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| **DIGITAL SYSTEM DESIGN LABORATORY** |
| **LAB 3** |

**IMPLEMENTATION OF BASIC COMBINATION LOGIC CIRCUIT USING VHDL**

### I. LAB OBJECTIVES

### This Lab experiments are intended to implement Basic Combination Logic and Sequential Circuit in VHDL. Students are require to write test bench to simulate the given example code and Top level module to implement these codes in DE2-115 FPGA Kit.

### a) For each experiment write the VHDL Code in three method ( dataflow, behavior and gate level)

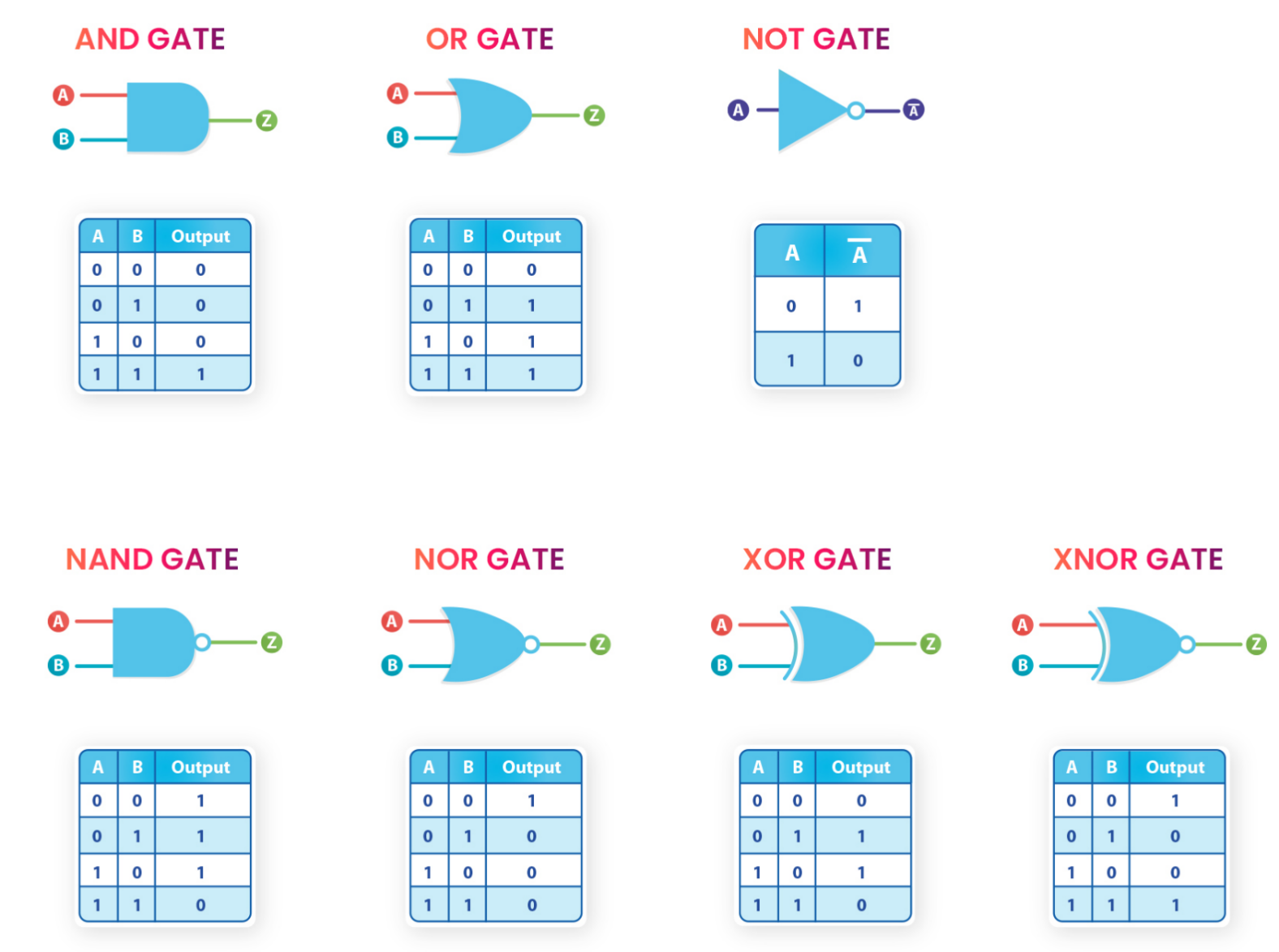
### b) For each model, write the Top Level VHDL Code to implement the these modules in DE2-FPGA Kit

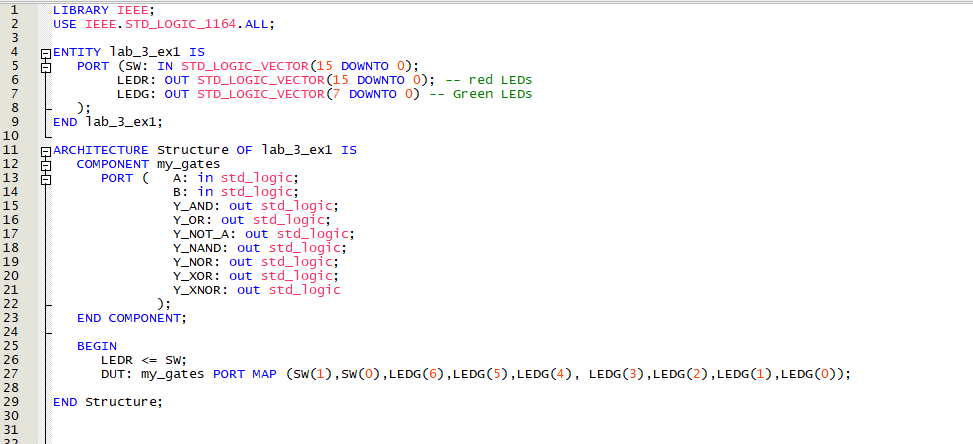
### (Show implementation results in Lab report)

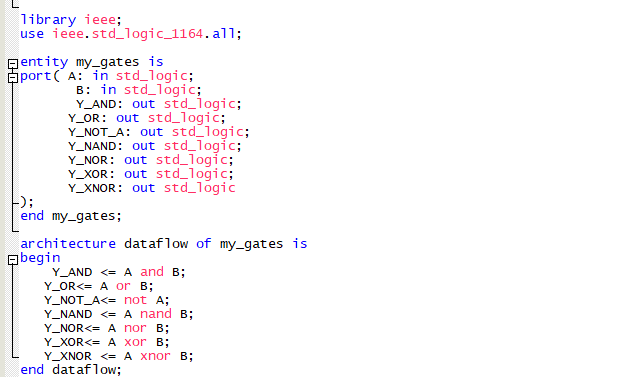
### c) Analyze the FPGA implementation results for these model

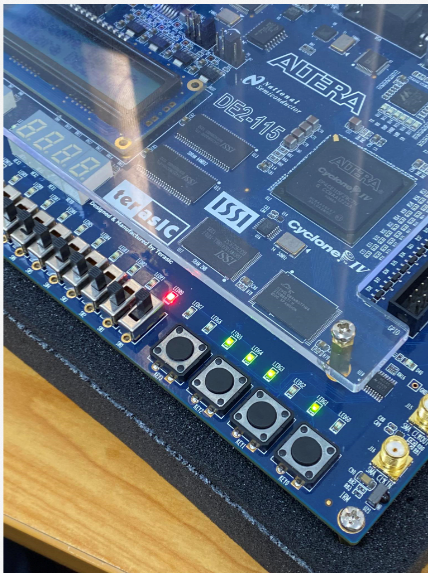
### II. PROCEDURE

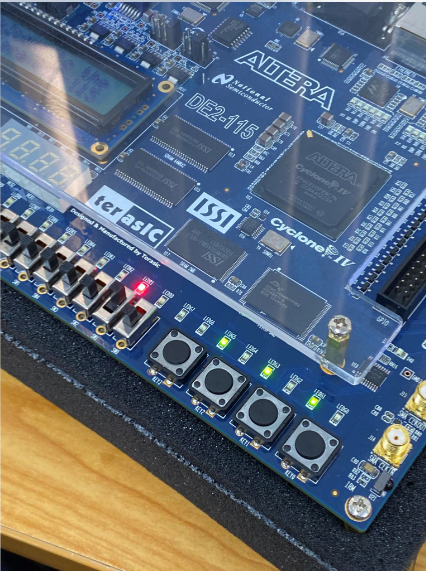
### II.1 LAB EXPERIMENT 1 : WRITE VHDL CODE TO IMPLEMENT ALL LOGIC GATES IN FPGA KIT.









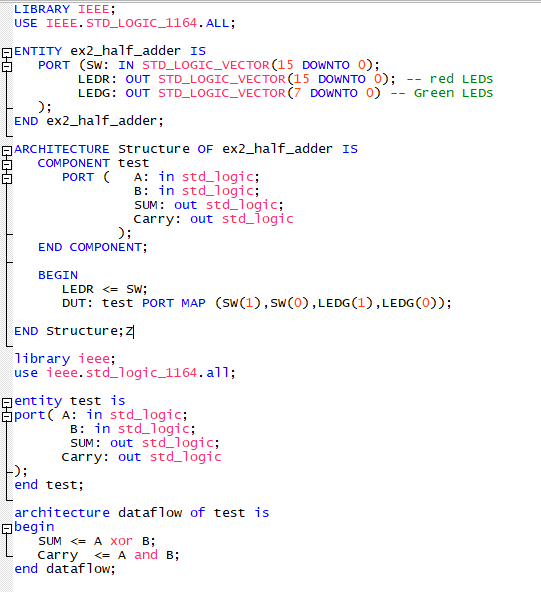


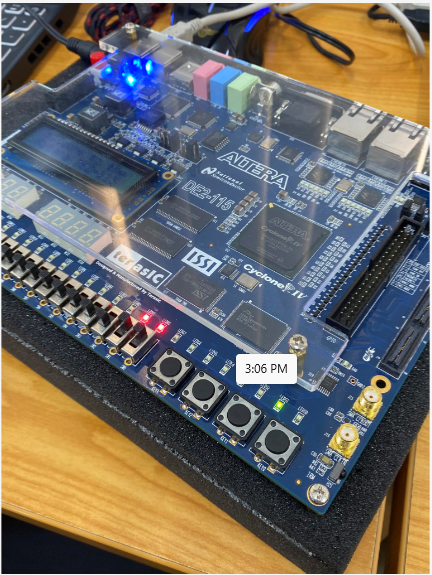
**II.2 LAB EXPERIMENT 2 : WRITE VHDL CODE TO IMPLEMENT THE HALF ADDER CIRCUIT IN FPGA KIT:**

A black line drawing of a circuit

Description automatically generated A table with numbers and symbols

Description automatically generated



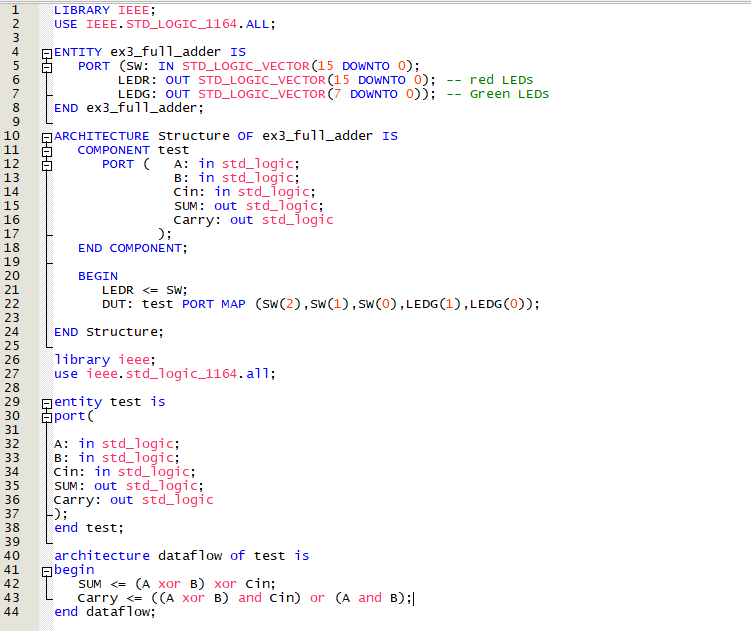


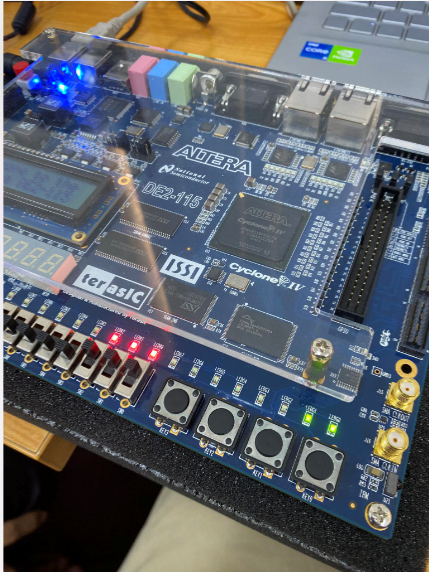
**II.3 EXPERIMENT 3: WRITE VHDL CODE TO SIMULATE AND IMPLEMENT THE FULL ADDER CIRCUIT IN FPGA KIT:**

**A diagram of a circuit

Description automatically generated A table of input output

Description automatically generated**



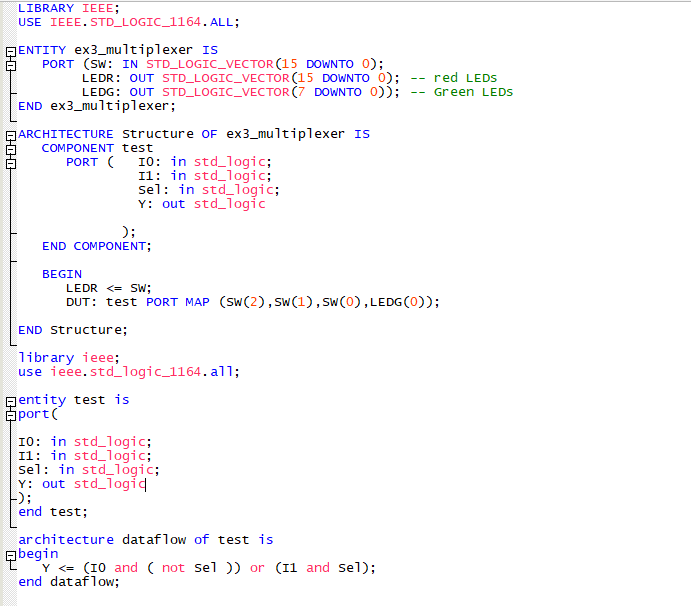


**II.4 EXPERIMENT 4 :WRITE VHDL CODE TO IMPLEMENT 2:1 MULTIPLEXER CIRCUIT IN FPGA KIT :**

A diagram of a network

Description automatically generated A square with black text

Description automatically generated with medium confidence



**II.5 EXPERIMENT 5 : WRITE VHDL CODES TO IMPLEMENT 4:1 MULTIPLEXER CIRCUIT IN FPGA KIT:**

A diagram of a circuit

Description automatically generated A diagram of a diagram and a diagram of a diagram

Description automatically generated

**II.6 EXPERIMENT 6 : WRITE VHDL CODE TO IMPLEMENT 2 to 4 DECODER CIRCUIT IN FPGA KIT:**

A diagram of a decoder

Description automatically generated

**II.7 EXPERIMENT 7 : WRITE VHDL CODE TO IMPLEMENT 8 TO 3 ENCODER WITH PRIORITY CIRCUIT IN FPGA KIT:**

A table with numbers and symbols

Description automatically generated

**II.8 EXPERIMENT 8 : WRITE VHDL CODES TO IMPLEMENT 1 TO 8 DEMULTIPLEXER CIRCUIT IN FPGA KIT:**

A diagram of a block diagram

Description automatically generated

A table with numbers and symbols

Description automatically generated

**II.9 EXPERIMENT 9 : WRITE VHDL CODES TO IMPLEMENT N-BIT COMPARATOR CIRCUIT IN FPGA KIT WITH FOLLOWING VHDL REFERENED CODE**

library ieee;

use ieee.std\_logic\_1164.all;

entity Comparator is

generic(n: natural :=4);

port( A: in std\_logic\_vector(n-1 downto 0);

B: in std\_logic\_vector(n-1 downto 0);

less: out std\_logic;

equal: out std\_logic;

greater: out std\_logic

);

end Comparator;

architecture behv of Comparator is

begin

process(A,B)

begin

if (A>B) then

less <= '0';

equal <= '0';

greater <= '1';

elsif (A=B) then

less <= '0';

equal <= '1';

greater <= '0';

else

less <= '1';

equal <= '0';

greater <= '0';

end if;

end process;

end behv;

**II.10 EXPERIMENT 10 : WRITE VHDL CODES TO IMPLEMENT N-BIT ALU CIRCUIT IN FPGA KIT WITH FOLLOWING VHDL REFERENED CODE**

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

entity ALU is

generic(N: natural :=4);

port( A: in std\_logic\_vector(N-1 downto 0);

B: in std\_logic\_vector(N-1 downto 0);

Op: in std\_logic\_vector(2 downto 0);

Res: out std\_logic\_vector(N-1 downto 0)

);

end ALU;

architecture behv of ALU is

begin

process(A,B,Op)

begin

case Op is

when "000" =>

Res <= A + B;

when "001" =>

Res <= A - B;

when "010" =>

Res <= not A ;

when "011" =>

Res <= not (A and B);

when “100” =>

Res <= not (A or B);

when “101” =>

Res <= A and B;

when “110” =>

Res <= A or B;

when “111” =>

Res <= A exor B;

end case;

end process;

end behv;

**IV. LAB REPORT GUIDELINES**

Students write up a report on the Verilog HDL implementation experiment projects created in this lab. The lab report should include Circuit Schematics, Truth Table, Verilog Module Codes, Verilog test bench codes, Top level module to implement the required circuit in FPGA KIT and evidences of data output evidences to validate the experiments (The Captured Screens, Photo of FPGA Kit implementation results).